Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method of piping defect detection comprising following steps:
providing a sample, the sample comprising:
a silicon substrate;
a plurality of electric devices disposed on the silicon substrate, the plurality of electric devices comprising a gate;
a dielectric layer covering the plurality of electric devices and the silicon substrate, the dielectric layer having a plurality of contact holes disposed on each of the electric devices, wherein at least a void is formed between two adjacent gates due to low uniformity of the dielectric layer coverage; and
a polysilicon layer covering the dielectric layer and electrically connecting to the electric devices through the contact holes, wherein the polysilicon film fills the contact holes to form a plurality of contact plugs and fills the void to form a piping defect;
performing a chemical mechanical polishing (CMP) process to remove the polysilicon layer and over polish the dielectric layer;
performing a wet etching process to etch the dielectric

layer selectively; and

inspecting the sample with a light source to search for the piping defect, wherein the polysilicon layer appear-sopaque but the dielectric layer appears transparent under the light source.

[c2] 2.The method of claim 1 wherein the chemical mechanic polishing process is performed until the contact plugs are not overlapping above the gates.

[c3] 3.The method of claim 1 wherein the light source comprises ultraviolet (UV) light.

[c4] 4.The method of claim 3 wherein the ultraviolet light comprises broadband UV light or narrowband UV light.

[c5] 5.The method of claim 1 wherein each of the electric devices is a MOS transistor, each MOS transistor comprising a gate disposed on the surface of the substrate, and further comprising a source and a drain disposed on both sides of the gate.

[c6] 6.The method of claim 1 wherein the dielectric layer comprises a borophospho-tetra-ethyl-otho silicate (BPTEOS) layer.

[c7] 7.The method of claim 1 further comprising performing a defect classification by utilizing an automatic defect

classification (ADC) tool.

[c8] 8.The method of claim 1 further comprising reviewing with a scanning electron microscope (SEM) after finding the location of the piping defect for analyzing the piping defect in advance.

[c9] 9.A method of defect detection for a semiconductor wafer, the method comprises following steps:
providing a semiconductor wafer comprising:
a silicon substrate; and
a dielectric layer positioned on the silicon substrate;
performing a pretreatment process to remove parts of the dielectric layer; and
inspecting the semiconductor wafer under ultraviolet light irradiation and judging the existence of the defect in the dielectric layer according to brightness differences in the image of the semiconductor wafer.

[c10] 10.The method of claim 9 wherein when a piping defect is present in the dielectric layer, a high brightness image is formed in the region of the piping defect under UV light irradiation.

[c11] 11. The method of claim 9 wherein the defect has a line width less than 0.1μm.

[c12] 12.The method of claim 9 wherein the pretreatment pro-

cess comprises a chemical mechanic polishing process and a wet etching process.

[c13] 13.The method of claim 9 wherein the semiconductor wafer further comprises a plurality of electric devices disposed on the surface of the silicon substrate.

[c14] 14.The method of claim 9 wherein the dielectric layer comprises a borophospho-tetra-ethyl-otho silicate (BPTEOS) layer.

[c15] 15.The method of claim 9 wherein the ultraviolet light comprises broadband UV light or narrowband UV light.

[c16] 16.The method of claim 9 further comprising performing a defect classification by utilizing an automatic defect classification (ADC) tool.

[c17] 17.The method of claim 9 further comprising reviewing with a scanning electron microscope (SEM) after finding the location of the defect for analyzing the found defect in advance.